Chemical vapor deposition and deep level analyses of 4H-SiC(11(2)over-bar0)

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Chemical vapor deposition and deep level analyses of 4H-SiC(11$\bar{2}$0)

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(Received 4 December 2000; accepted for publication 7 March 2001)

Specular 4H-SiC layers have been homoepitaxially grown on 4H-SiC(11$\bar{2}$0), parallel to the *c* axis (⟨0001⟩), by chemical vapor deposition at 1500 °C. An x-ray diffraction analysis has revealed that a lattice-mismatch strain between n^- epilayers and n^+ substrates could be minimized by introducing *n*-type buffer layers. The donor concentration of unintentionally doped epilayers could be reduced down to $1\times10^{14}\,\mathrm{cm}^{-3}$ under a C-rich growth condition. Through isothermal capacitance transient spectroscopy measurements, three acceptor-like traps with activation energies of 0.27, 0.32, and 0.66 eV have been detected with a total trap concentration as low as $3.8\times10^{12}\,\mathrm{cm}^{-3}$. The capture cross section of the deepest trap, the Z_1 center, at high temperatures has been determined.
 [DOI: 10.1063/1.1368863]

I. INTRODUCTION

Unique potential of silicon carbide (SiC) has been demonstrated in various prototype devices projected for high-power, high-frequency, and high-temperature electronics.[1] It has been revealed, however, that micropipes, hollow cores associated with superscrew dislocations propagating along the ⟨0001⟩ (*c*-axis) direction, cause premature breakdown in high-voltage SiC devices.[2] Although the micropipe density of SiC wafers has significantly been reduced in the last several years,[3] commercial SiC wafers still contain a few tens of micropipes/cm^2, and the elemental screw dislocations existing in a much higher density of 10^3 to $10^4\,\mathrm{cm}^{-2}$ may also affect device performance.[4,5]

Recently, Takahashi and coworkers have succeeded in producing ''micropipe-free'' SiC wafers by sublimation growth on (1$\bar{1}$00) and (11$\bar{2}$0) seed crystals.[6,7] These SiC(1$\bar{1}$00) and (11$\bar{2}$0) wafers with surface orientation parallel to the *c* axis have much potential for developing large-area SiC devices, leading to the increased current (or power) handling capability. However, only a few works have been reported concerning SiC epitaxial growth on 4H- or 6H-SiC(11$\bar{2}$0) and (1$\bar{1}$00) substrates.[8–10] The quality of SiC(11$\bar{2}$0) epilayers and doping control have not been fully investigated. The authors have reported successful homoepitaxy of 4H-SiC(11$\bar{2}$0) by chemical vapor deposition (CVD),[11,12] and realized high-voltage Schottky barier diodes with reduced leakage current.[12] In 1999, the authors have also found that the channel mobility of 4H-SiC inversion-type metal–oxide–semiconductor field effect transistors (MOSFETs) can be remarkably improved up to 96 cm^2/V s by utilizing (11$\bar{2}$0), compared to 5 to 6 cm^2/V s on the conventional off-axis (0001).[13]

In this article, details of epitaxial growth and systematic characterization of 4H-SiC(11$\bar{2}$0) are presented. Advantages and remaining issues of 4H-SiC(11$\bar{2}$0) epitaxial growth are also discussed.

II. EXPERIMENTS

Homoepitaxial growth was performed by atmospheric-pressure CVD in a cold-wall horizontal reactor.[14] Source gases were SiH_4 and C_3H_8 with a Pd-cell purified H_2 carrier gas. Typical flow rates were 0.30 sccm, 0.20–0.50 sccm, and 3.0 slm, for SiH_4, C_3H_8, and H_2, respectively. The *n*-type 4H-SiC(11$\bar{2}$0) substrates with a doping concentration in the $10^{18}\,\mathrm{cm}^{-3}$ range were prepared by cutting parallel to (11$\bar{2}$0) faces from [000$\bar{1}$] grown ingots at Nippon Steel Corp. The (11$\bar{2}$0) substrates were nominally ''on-axis'' with possible off-angles less than 0.5°. For comparison, the 8° off-axis 4H-SiC(0001) substrates were placed side by side on an SiC-coated susceptor in a CVD reactor. Typical growth temperature and growth rate were 1500 °C and 2.5 μm/h, respectively. *In situ* HCl etching was carried out at 1300 °C for 10 min to remove surface damage introduced during polishing processes. Under a typical growth condition, the growth rate on (11$\bar{2}$0) was nearly identical to that on off-axis (0001), because the growth on both faces is diffusion controlled.[12,14]

Epilayers were characterized by a Nomarski microscope, atomic force microscopy (AFM), x-ray diffraction, and photoluminescence. Electrical properties were assessed by capacitance–voltage ($C-V$) and isothermal capacitance transient spectroscopy (ICTS)[15] measurements on a Ni/4H-SiC Schottky structure. In the ICTS, deep trap signals are detected by the transient time scan, instead of the temperature scan as in deep level transient spectroscopy (DLTS). ICTS spectra were typically acquired on 1.2 mmϕ Schottky diodes with a reverse bias voltage of −5 V, a pulse voltage of 5 V, and a pulse width of 20 ms, if not specified.

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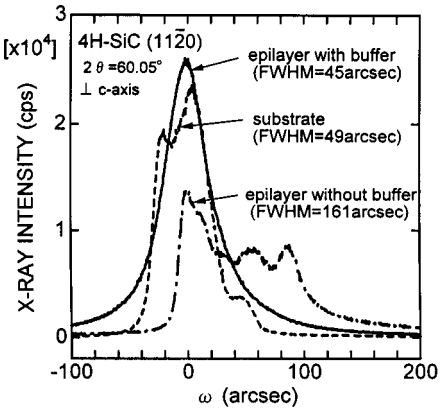

FIG. 1. X-ray rocking curves at the SiC(11$\bar{2}$0) peak ($2\theta=60.05°$) obtained from 9-μm-thick n^--type 4H-SiC(11$\bar{2}$0) epilayers grown on n^+-type substrates with or without a buffer layer, and from a substrate.

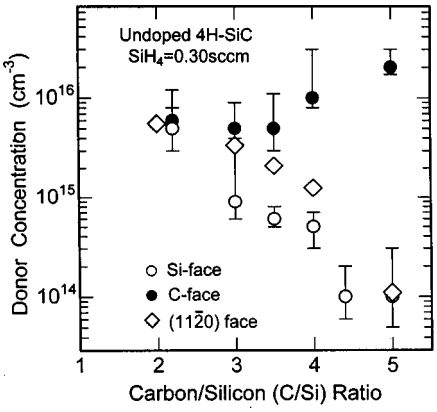

FIG. 2. C/Si ratio dependence of donor concentration for unintentionally doped 4H-SiC epilayers grown on off-axis 4H-SiC (0001), off-axis (000$\bar{1}$), and on-axis (11$\bar{2}$0) substrates.

III. RESULTS AND DISCUSSION

The 4H-SiC(11$\bar{2}$0) epilayers exhibited very good morphology and a small surface roughness of 0.18 nm without any triangular defects and ''carrot-like'' grooves which occasionally appear on off-axis SiC(0001) epilayers. On off-axis SiC(0001) substrates, homoepitaxy is realized through step-flow growth.[14] In contrast, no signs of ''step-flow'' such as step bunching have been observed for SiC(11$\bar{2}$0) epilayers, suggesting two-dimensional nucleation and subsequent layer-by-layer growth. Takahashi and Ohtani reported the perfect polytype replication in sublimation growth on 4H- and 6H-SiC(11$\bar{2}$0) seeds.[7] As illustrated by Takahashi and Ohtani[7] and Chen *et al.*,[11] the unique stacking sequence of SiC polytype appears on the SiC(11$\bar{2}$0) face, which ensures very little or no opportunity for adatoms to be incorporated at a misarranged lattice site. This may be the reason why no off-angle is required for SiC homoepitaxy on (11$\bar{2}$0). It should be noted that the use of this face is effective for homoepitaxy at low temperatures below 1350 °C.[8]

Figure 1 depicts x-ray rocking curves (ω scan) sensitive to lattice tilt and crystal bending, at the (11$\bar{2}$0) peak ($2\theta=60.05°$) obtained from 9-μm-thick n^--type 4H-SiC(11$\bar{2}$0) epilayers grown on n^+-type substrates with or without a buffer layer, and from a substrate. The epilayer directly grown on a substrate without a buffer layer exhibited considerable broadening of the diffraction peak with splitting [FWHM (full width at half maximum) = 161 arcsec]. Similar degradation of epilayer quality (FWHM > 200 arcsec) has been pointed out in 4H-SiC(1$\bar{1}$00) and (11$\bar{2}$0) growth by hot-wall CVD.[9] This peak broadening may originate from a lattice-mismatch strain caused by the doping difference between an n^- epilayer and an n^+-substrate.[9] Since this problem is not pronounced on an off-axis (0001) face, the lattice-mismatch strain caused by the doping difference may be more stringent for a (11$\bar{2}$0) face. By introducing a 1.2-μm-thick *n*-type buffer layer with a four-step stair-like doping profile from 5×10^{17} to 1×10^{16} cm^{-3}, the FWHM of rocking curve could be improved to 45 arcsec, being even smaller than the substrate (49 arcsec).

From molten KOH etching at 450 °C for 10 min, 4H-SiC(11$\bar{2}$0) epilayers turned out to be micropipe free. Instead, triangular etch pits related to dislocations[9] with a density of 10^4 cm^{-2} were observed. The exact defect structure responsible for these etch pits is not known at present. The stacking fault density was estimated to be in the 10^2 cm^{-1} range. All the stacking faults existing in substrates seem to be replicated in (11$\bar{2}$0) epilayers. In some cases, a smooth epilayer surface was abruptly disturbed by stripe-like morphology on the area where a high density of stacking faults is localized. The effects of stacking faults on SiC device performance should be clarified in order to bring 4H-SiC(11$\bar{2}$0) into real applications.

The dependence of the donor concentration on the C/Si ratio for unintentionally doped 4H-SiC epilayers on various substrate faces is represented in Fig. 2. The doping concentration on (11$\bar{2}$0) is sensitive to the C/Si ratio, following the site-competition concept,[16] and is located in between that on (0001) Si and (000$\bar{1}$)C faces. The lowest net donor concentration determined from $C-V$ measurements was 1.1×10^{14} cm^{-3}, which was obtained by increasing the C/Si ratio up to 5 (Fig. 2). In spite of this C-rich CVD condition, surface morphology was still excellent, suggesting a wide growth window on the (11$\bar{2}$0) face. With respect to intentional nitrogen or aluminum doping, the doping efficiencies on the (11$\bar{2}$0) face were also located in between that on (0001) Si and (000$\bar{1}$)C faces.[17] Our CVD experiments on (11$\bar{2}$0) result in higher donor concentration for nitrogen-doped epilayers and lower acceptor concentration for boron-doped epilayers by a factor of 2–5, compared to off-axis (0001) epilayers grown in the same CVD run.

In low-temperature photoluminescence at 18K for lightly doped 4H-SiC(11$\bar{2}$0) epilayers, well-resolved peaks due to the recombination of excitons bound to neutral nitrogen donors and free exciton peaks were observed. Note that because of the indirect band structure of SiC only phonon replicas of free-exciton recombination appeared. Above 40–50 K, the nitrogen-donor bound exciton peaks are quenched, making the free exciton peaks dominant. The free exciton peaks sur-

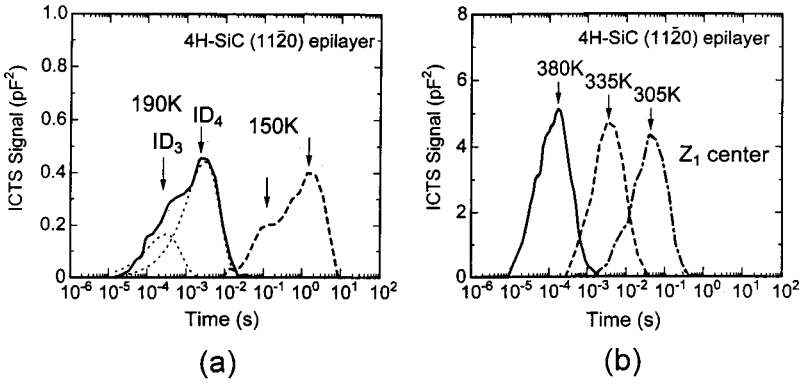

FIG. 3. ICTS spectra from a 15-μm-thick 4H-SiC (11$\bar{2}$0) epilayer in the (a) low-temperature and (b) high-temperature ranges.

vived even at 290 K, indicating high purity of epilayers. At 290 K, free exciton peaks were strongly broadened due to the increased thermal energy of excitons and to the overlapping of a few phonon replicas.

The authors have investigated deep levels in 4H-SiC(11$\bar{2}$0) epilayers by ICTS. Wide range scans of both temperature (120–420 K) and transient time (10^{-6}–10^{4} s) in ICTS measurements on high-purity epilayers ($N_d = 1 \times 10^{14}\,\mathrm{cm}^{-3}$) enabled very high-resolution detection in the energy range from $E_C - 0.1$ eV (E_C is the bottom of the conduction band) down to about $E_C - 1.3$ eV (close to midgap). Figure 3 represents typical ICTS spectra from a 15-μm-thick 4H-SiC(11$\bar{2}$0) epilayer in the (a) low-temperature and (b) high-temperature range. The ordinate shows the ICTS signal $S(t)$ defined by $t \cdot dC^2(t)/dt$ [$C(t)$ is the transient capacitance and t is the time].[15,18] One double peak was observed in the low-temperature measurements [Fig. 3(a)], where theoretical fitting curves for the ICTS spectra at 190 K are plotted by dotted curves. Although one main peak and two shoulders seem to exist for each ICTS spectrum, only two traps were sufficient to reproduce the spectrum with the corresponding theoretical curves at any temperature measured. However, the determination of emission time constants from the curve fitting may be inaccurate, especially for the smaller peak (the faster trap). On the other hand, one single peak appeared at high temperatures as shown in Fig. 3(b). No other ICTS peaks were detected at higher temperatures and longer transient times. The Arrhenius plots of emission time constants (τ) for three different traps are shown in Fig. 4, assuming a temperature-independent capture cross section, and the obtained trap parameters are summarized in Table I. The activation energies of detected traps were determined to be 0.27, 0.32, and 0.66 eV, respectively. The electric field dependence of emission time constants was examined by varying the reverse bias voltage from 0 V to −20 V, which corresponds to the change of average electric field strength from 1.2×10^3 to 1.3×10^4 V/cm. The emission time constants for the traps exhibited no electric field dependence within the uncertainty of the measurement (±3%). This result means the lack of Poole–Frenkel effect, suggesting that all the traps observed are acceptor-like (0/−). Considering the activation energy, the capture cross section, the charge state, and thermal stability, the observed traps can be assigned to the ''ID$_3$,'' ''ID$_4$,'' and ''Z$_1$'' centers,[19] respectively. So far, intrinsic defect complexes have been suggested as the origins of these traps.[19] It should be noted, however, that the total trap concentration is as low as $3.8 \times 10^{12}\,\mathrm{cm}^{-3}$ and is favorably compared to that observed for 4H-SiC(0001) epilayers (4×10^{12}–$1 \times 10^{13}\,\mathrm{cm}^{-3}$).[14,20,21] In photoluminescence measurements, the L_1 peak at 427.2 nm, which has been supposed to have the same origin as the Z$_1$ center,[22] was very difficult to observe, probably due to the very low defect concentration.

Figure 5 represents the depth profiles of trap concentrations for the ID$_3$, ID$_4$, and Z_1 centers observed from a 15-μm-thick 4H-SiC(11$\bar{2}$0) epilayer, which were deduced from the bias voltage dependence of ICTS spectra. By changing the reverse bias voltage from 0 to −20 V, the width (depth)

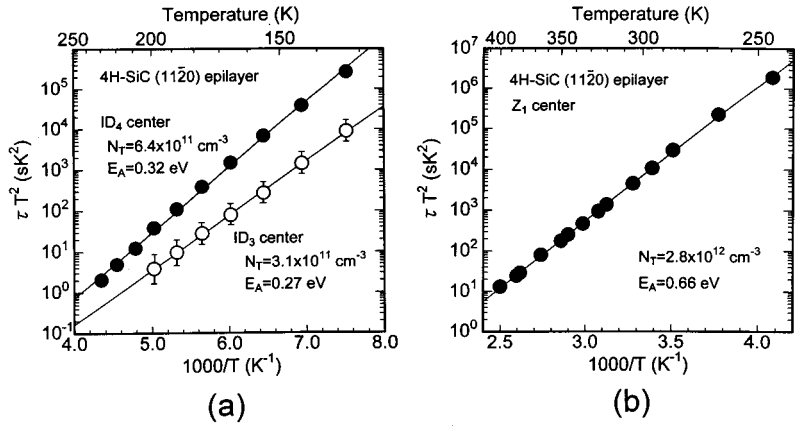

FIG. 4. Arrhenius plots of emission time constants (τ) for (a) two shallow traps and (b) a deep trap observed in 4H-SiC(11$\bar{2}$0) epilayers, assuming temperature-independent capture cross section.

TABLE I. Trap parameters of defect centers observed in as-grown 4H-SiC($11\bar{2}0$) epilayers.

Center	Activation energy (eV)	Capture cross section (cm^2)	Concentration (cm^{-3})
ID_3	0.27	4×10^{-16}	3.1×10^{11}
ID_4	0.32	1×10^{-15}	6.4×10^{11}
Z_1	0.66	4×10^{-15}	2.8×10^{12}

of the space charge region monitored was modulated. All the trap concentrations tend to decrease toward the epilayer surface. The authors have observed the continuous decrease in the background impurity concentration for undoped SiC epilayers with increasing the epilayer thickness, owing to a ''baking effect.'' It has been supposed, however, that all the ID_3, ID_4, and Z_1 centers do not contain specific impurity atoms.[19] Further investigations are required to understand the gradual reduction of trap concentration through thicker or longer-time epitaxial growth.

The authors have measured the capture cross section of the Z_1 center at elevated temperatures by the pulse-filling technique[23] in ICTS. As in DLTS, the sufficiently narrow width of pulse voltage in ICTS measurements resulted in the ''reduced'' trap concentration, because only a limited portion of traps can capture electrons during the short filling pulse. The concentration of electrons (n_T) trapped by a deep level in a short pulse measurement is given by[23]

$$n_T = N_T\{1-\exp(-\sigma n v_{th} t_p)\}. \quad (1)$$

Here, N_T is the real trap concentration determined from a sufficiently long (>20 ms) filling pulse measurement, $v_{\rm th}$ is the thermal velocity of an electron, σ is the capture cross section, n is the free electron concentration, and t_p is the width of filling pulse. Typical results of this technique for the Z_1 center in 4H-SiC are demonstrated in Fig. 6, where the $\log(1-n_T/N_T)$ versus the pulse width t_p is plotted. In the present study, the high purity of 4H-SiC epilayers ($n\sim1\times10^{14}\,cm^{-3}$) enabled reasonably long-pulse width measurements in the 10^{-6} s range, ensuring the accuracy of this measurement. For the data at all the measurement temperatures, the intercepts in the vertical axis by extrapolating the plots

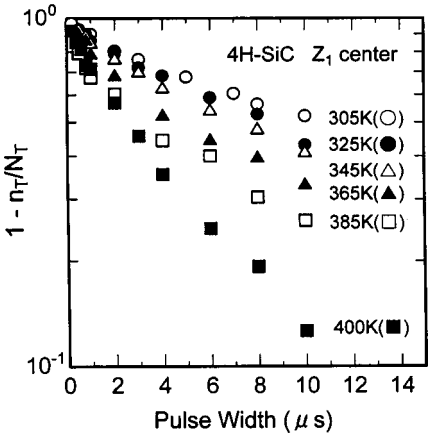

FIG. 6. $\log(1-n_T/N_T)$ vs pulse width t_p plots for the Z_1 center in 4H-SiC at various temperatures.

toward the zero pulse width are close to unity, as is expected from Eq. (1). The slope in this extrapolation provides the information of capture cross section. The temperature dependence of capture cross section for the Z_1 defect center is represented in Fig. 7. The recent data in the low-temperature range reported by Hemmingsson *et al.* are also shown.[24] The least-square fitting of the present data gives the following equation.

$$\sigma(Z_1\ \text{center}) = 9.4\times10^{-16}\ \exp(-0.074\ eV/kT)\ [\text{cm}^2]. \quad (2)$$

This exponential relationship at high temperatures indicates that electrons are captured through a multiphonon process.[23] The present data show good agreement with those extrapolated from the values measured at lower temperatures.[24] Hemmingsson *et al.* have reported that the Z_1 center eventually consists of two centers which have very close activation energies and capture cross sections.[24] This is the reason why two dotted lines are displayed as references in Fig. 7. In this study, however, it was difficult to resolve the observed ''single'' ICTS peak of the Z_1 center into two overlapping peaks. As seen from Fig. 7, the difference of the capture cross section for two centers becomes smaller at elevated temperatures. This decreased difference of trap parameters at

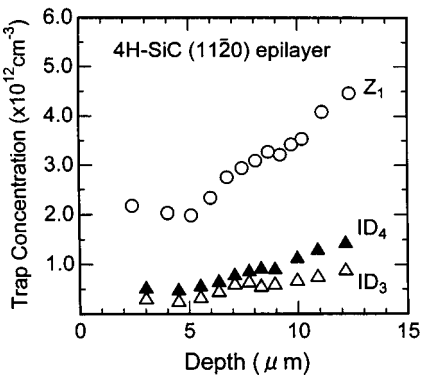

FIG. 5. Depth profiles of trap concentrations for the ID_3, ID_4, and Z_1 centers observed from a 15-μm-thick 4H-SiC($11\bar{2}0$) epilayer, which were deduced through the bias voltage dependence of ICTS spectra.

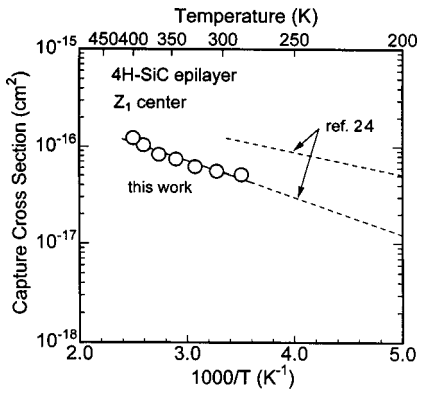

FIG. 7. Temperature dependence of capture cross section for the Z_1 defect center in 4H-SiC, together with the recent data reported by Hemmingsson *et al.* (see Ref. 24).

elevated temperatures may have affected the peak separation of the Z_1 center in the present measurements. However, it is noteworthy that this work provides the measurement of the capture cross section at high temperatures, which may be of more importance for device applications.

IV. CONCLUSIONS

CVD growth and characterization of 4H-SiC$(11\bar{2}0)$ epilayers were investigated. Owing to the appearance of peculiar stacking sequence on the surface, homoepitaxy of 4H-SiC could be realized on on-axis $(11\bar{2}0)$ substrates. The $(11\bar{2}0)$ epilayers showed very smooth morphology, and the quality could be improved by introducing an *n*-type buffer layer to minimize lattice-mismatch strain between an n^- epilayer and an n^+ substrate. The lowest donor concentration of unintentionally doped epilayers is $1\times10^{14}\,\mathrm{cm}^{-3}$, which was achieved by increasing the C/Si ratio up to 5. Both the dependence of impurity doping on the C/Si ratio and the doping efficiency on the $(11\bar{2}0)$ face are located in between those on the (0001)Si and $(000\bar{1})$C faces. ICTS measurements revealed three electron traps located at $E_C-0.27$, 0.32, and 0.66 eV with a total trap concentration as low as $3.8\times10^{12}\,\mathrm{cm}^{-3}$. All the trap concentrations showed a decreasing profile toward the epilayer surface. The capture cross section of the Z_1 center at elevated temperatures from 280 to 400 K was determined. The present study together with attractive MOSFET performance[13] indicates that micropipe-free 4H-SiC$(11\bar{2}0)$ epilayers with proper buffer layers are a promising alternative for high-power SiC device applications. Reduction of stacking faults and the production technology of large-area 4H-SiC$(11\bar{2}0)$ wafers will be critical remaining issues.

ACKNOWLEDGMENTS

The authors express gratitude to Dr. N. Ohtani at Nippon Steel Corp. for supplying 4H-SiC$(11\bar{2}0)$ substrates. They are also grateful to Professor I. Kimura and Dr. S. Kanazawa at Department of Nuclear Engineering, Kyoto University, for the use of ICTS equipment. This work was partially supported by a Grant-in-Aid for Specially Promoted Research, No. 09102009, from the Ministry of Education, Science, Sports and Culture, Japan, and NEDO. Kyoto University Venture Business Laboratory is also acknowledged.

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